# FPGA coprocessors for acceleration of shape algorithms in hybrid VPX HPEC systems























# Shape Recognition Research Program

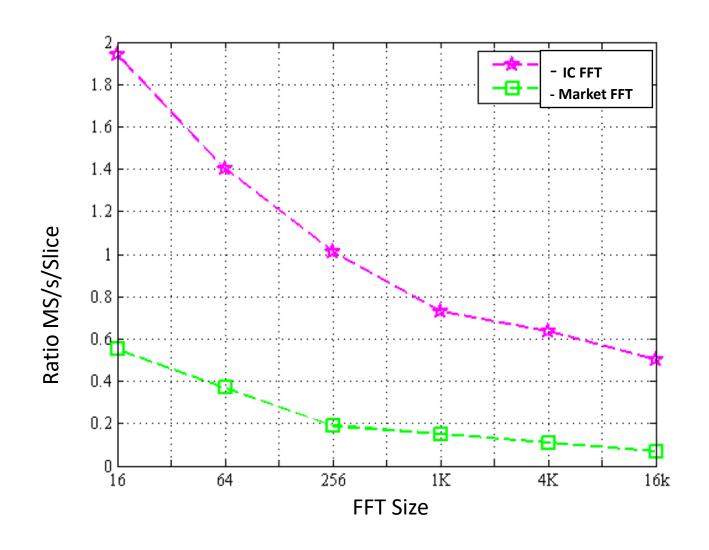
- IC part of a R&D program with the EBO University in Brittany for shape recognition algos running in FPGAs
- First part of the program was about developing new innovative implementations in FPGA of Fast Fourrier Transform (FFT) and Discrete Cosine Transform (DCT) leading to:
  - Reduction in execution time
  - Decrease of the FPGA resources

# Shape Recognition FFT Performances

- Achievement in improving FFT performances compared to the IP on the market:
  - Improvement by a factor of 5 of the ratio throughput versus the number of slices for a 256 FFT
  - Improvement by a factor of 4 of the ratio throughput versus the number of slices for a 16K FFT
- Power for execution in a continuous mode of:
  - 1024 points FFT in a Virtex-6 FPGA: 100 mW
  - 4096 points FFT: 150 mW
  - 64 points FFT: 50 mW.



# Shape Recognition FFT Performances





## Shape Recognition Algorithm

- Second part of the program consisted in using the improved FFT and build a high speed shape recognition algorithm
- Base of the Shape Recognition Algorithm:
  - Processing of a digital correlation between a target image and a reference image.
  - This correlation is carried out:
    - By multiplying the spectrums of the target image and the reference image (using a 2D FFT to get the spectrums of the images),
    - Then taking the inverse 2D FFT of the result.
    - Energy of the correlation peak normalized to the total energy of the correlation plan



## Shape Recognition Algorithm

#### Achievements:

- One XC7VX690T can simultaneously support around 30 correlation architectures described above, each correlation architecture being able to process around 4, 000 images per second.
- One XC7VX690T can process and decide on 120, 000 images per second.
- A VPX HPEC system with 5 dual Virtex-7 boards IC-FEP-VPX6b, each one connected to two 12 x 10GbE optical FMC IC-OPT-FMCa can process 1.2 Mega images per second





## Last generation of FPGAs



#### Example with the VU13P UltraScale+:

- 3.5 Million of logic cells (Factor of 5 compared to XC7VX690T and up to 12 K DSP enhanced slices-factor of 4)
- 128 32.25 Gb/s transceivers and multi terabit per second throughput
- Integrated 100GE MAC blocks and PCIe Gen3 cores
- Advanced clock management, distributed clock buffers allowing the processing of massive parallel applications with high width buses (typically 2048 bits)
- IC is currently designing new Ultrascale+ COTS boards to take benefit from these outstanding performances (IC-FEP-VPX6d/e)



# IC-OPT-FMCa in partnership with Reflex Photonics

- IC-OPT-FMCa supports the 2 FMC connectors:
  - VITA57.1 FMC HPC 10 full duplex optical link at up to 28Gbps each max
  - VITA 57.4 FMC HSPC 12 full duplex optical link at 28Gbps each max

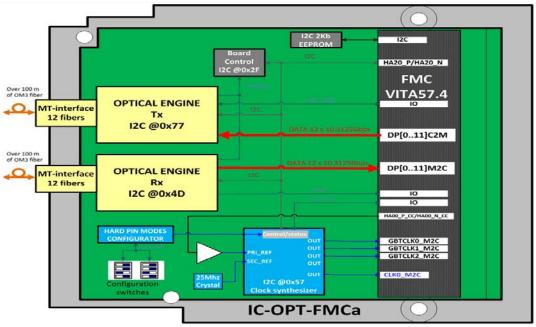


		Transportation of the contract		
		Car	Carrier	
		VITA 57.1	VITA 57.4	
F	VITA 57.1	Compatible	Compatible	
M C	VITA 57.4	N/A	Compatible	

\*

<sup>1</sup>\*





\*

